REMARKS/ARGUMENTS

Claims 1-20 are pending.

Applicants note with appreciation the indicated allowability of claim 17 if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 17 has not amended at this time because Applicants believe all the claims are patentable.

Claims 1-4, 6-10, 12-16, and 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Saiki et al. (US 5,677,802).

Applicants respectfully submit that independent claim 1 is novel and patentable over Saiki et al. because, for instance, Saiki et al. does not teach or suggest a read clock control means for controlling the phase of said read clock signal in accordance with the phase of said read signal read by said magnetic head to correct the phase of said read clock signal if a phase shift between said read clock signal and said read signal exceeds a predefined value. As discussed in the specification at page 10, lines 6-9, correction of the phase by the read clock control means occurs if the phase shift exceeds a predefined value.

In contrast, Saiki et al. discloses phase correction by the VCO circuit. The Examiner cites Saiki et al. at column 8, lines 23-46 for allegedly disclosing "if a phase shift between said clock signal and said read signal exceeds a predefined value." Saiki et al., however, merely states: "a PLL controller circuit for detecting the amount of phase shift from a signal 105 output by the EQ circuit 6 and outputting the amount of the phase shift as an error signal." Nothing in Saiki et al. discloses or suggests making the phase correction if the phase shift exceeds a predefined value.

In the Examiner's Response to Arguments, the Examiner alleges that "Saiki does teach comparing and discriminating the phase of a read signal with regards to a clock signal in a magnetic medium." This does not constitute teaching of making the phase correction if the phase shift exceeds a predefined value. The Examiner is respectfully requested to point out

where in Saiki et al. teaches **comparison of the phase shift to a predefined value** and where it teaches **making the phase correction if the phase shift exceeds a predefined value.**

Saiki et al. does not even disclose a comparison of the phase shift to a predefined value. While a comparison means is used in the comparison circuit 31 within the PLL controller circuit 7, the mere use of a comparison means is not equivalent to determining if a phase shift exceeds a predefined value. In column 8, lines 42-46, Saiki et al. recites that the comparison circuit "determin[es] whether the data 136 output by the [1+D] circuit 36 is either positive, zero or negative and output[s] "1", "0" or "-1" for a positive, zero or negative result of the detection of the data 136." The comparison circuit 31 is used to determine the sign of the input data, but it does not compare the input data to a predefined value. Nothing in Saiki et al. teaches or suggests such a comparison to a predefined value. Clearly, it does not teach making a phase correction if a phase shift between the read clock signal and the read signal exceeds a predefined value, as recited in independent claim 1.

For at least the foregoing reasons, independent claim 1 and claims 2-4, 6-8, and 16 depending therefrom are novel and patentable over Saiki et al.

Applicants respectfully assert that independent claim 9 is novel and patentable over Saiki et al. because, for instance, Saiki et al. does not teach or suggest a phase corrector configured to control said oscillator in accordance with the phase of said read signal, which is detected by said phase detector, in order to correct the phase of the read control signal generated by said oscillator if a phase shift between said read control signal and said read signal exceeds a predefined value. This is described in the specification at page 10, lines 21-23.

As discussed above, Saiki et al. discloses phase correction by the VCO circuit. Nothing in Saiki et al. discloses or suggests making the phase correction by a phase corrector if the phase shift exceeds a predefined value.

For at least the foregoing reasons, independent claim 9 and claims 10, 12, 18, and 19 depending therefrom are novel and patentable over Saiki et al.

Applicants respectfully contend that independent claim 13 is novel and patentable over Saiki et al. because, for instance, Saiki et al. fails to teach or suggest making corrections, if data is not successfully read due to a phase difference between said read clock signal and said read signal with said phase difference exceeding a predefined value, to adjust the phase of the read clock signal for the phase of the read signal.

As discussed above, Saiki et al. discloses phase correction by the VCO circuit. Nothing in Saiki et al. discloses or suggests making the phase correction if the phase shift exceeds a predefined value.

For at least the foregoing reasons, independent claim 13 and claims 14, 15, and 20 depending therefrom are novel and patentable over Saiki et al.

Claims 5 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Saiki et al. in view of Muto et al. (US 5,436,770). The Examiner recognizes that Saiki et al. does not disclose that the storage means is a register provided for the read/write channel, and cites Muto et al. for the missing feature.

Applicants note, however, that Muto et al. does not cure the deficiencies of Saiki et al. in that Muto et al. also fails to teach or suggest a read clock control means for controlling the phase of said read clock signal in accordance with the phase of said read signal read by said magnetic head to correct the phase of said read clock signal if a phase shift between said read clock signal and said read signal exceeds a predefined value, as recited in claim 1 from which claim 5 depends; and a phase corrector configured to control said oscillator in accordance with the phase of said read signal, which is detected by said phase detector, in order to correct the phase of the read control signal generated by said oscillator if a phase shift between said read control signal and said read signal exceeds a predefined value, as recited in claim 9 from which claim 11 depends.

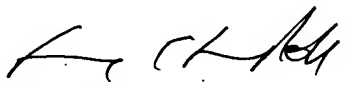
For at least the foregoing reasons, claims 5 and 11 are patentable over Saiki et al. and Muto et al.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
RL:dlw
60539440 v1